

700V Advanced GaN Power IC CYPG6148C

1. Features

- Integrated gate drive
- 3.3V/5V/15V PWM logic input compatible
- Programmable accurate GaN current sensing
- Over-temperature protection
- Wide V_{CC} range (10V to 24V typical)
- Low standby current (50uA typical)
- Sleep mode current (10uA max)
- Built-in turn-on dV/dt optimization
- Built-in turn-off di/dt optimization
- Reliable hard and soft switching
- Zero reverse recovery charge

DPAK-4L package with grounded cooling pad

- Grounded cooling pad
- Minimized package inductance
- Low thermal resistance

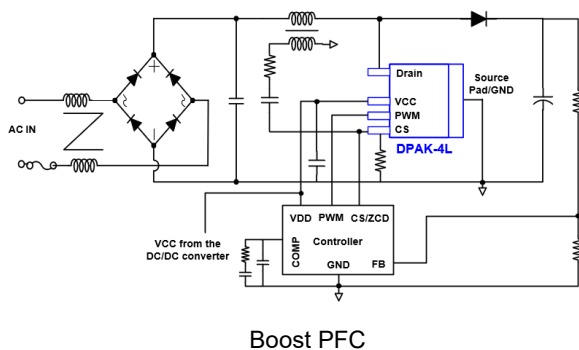
Sustainability

- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO2 Carbon Footprint reduction

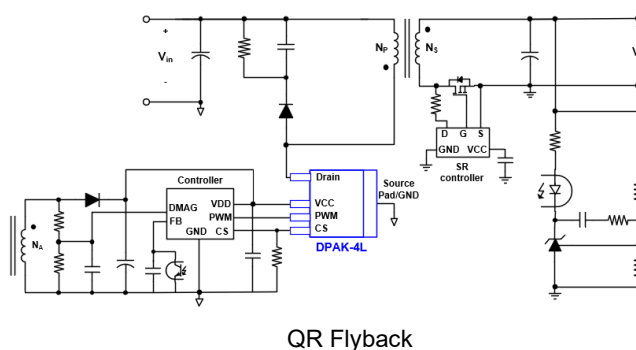
2. Applications

- AC-DC Charger & Adapter
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV Power
- Server Power, Telecom Power

4. Typical Application Circuits



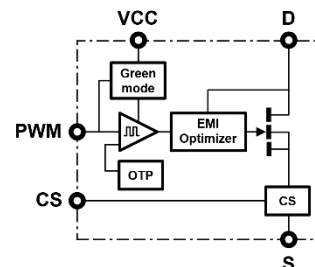
Boost PFC



QR Flyback



DPAK-4L



Simplified schematic

3. Description

This feature-rich 700 V GaN Power IC includes a high performance eMode GaN FET (120mΩ), integrated gate drive, and extended features to create the fastest, smallest, most efficient, and most robust integrated powertrain in the world.

Integrated lossless current sensing eliminates external current sensing resistors and increases system efficiency, over-temperature protection increases system robustness, auto standby and sleep mode increases light/tiny/no-load efficiency.

The highest dV/dt immunity, high-speed integrated drive and industry-standard low-profile, low-inductance, DPAK package combine to enable designers to exploit Cyient Semiconductors' GaN technology with simple, quick, reliable solutions achieving breakthrough power density and efficiency.

Cyient Semiconductors' GaN power ICs extend the capabilities of traditional topologies and enable the commercial introduction of breakthrough designs.

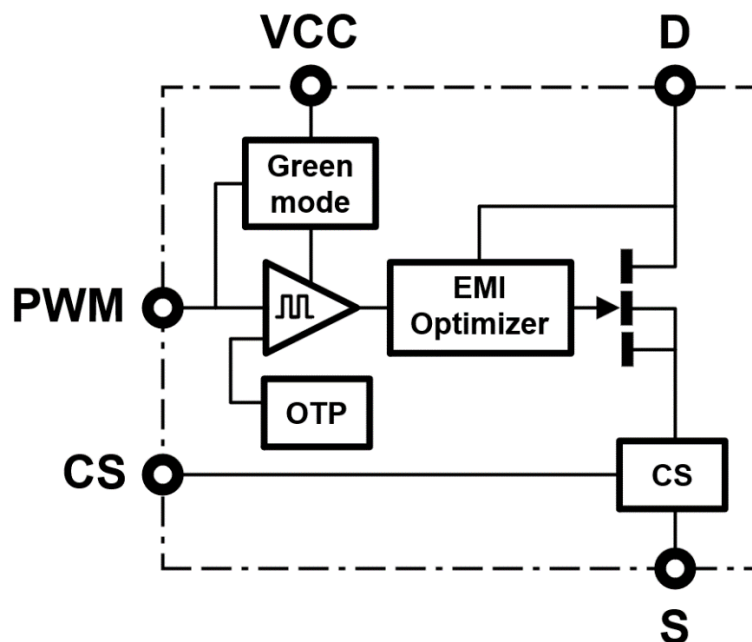


SEE IMPORTANT NOTICES AND DISCLAIMERS AT THE END OF THIS DATA SHEET REGARDING THE INFORMATION IN THIS DATA SHEET, THE USE OF OUR PRODUCTS, AND YOUR RESPONSIBILITIES RELATING TO SUCH USE.

5. Table of Contents

1. Features	1
2. Applications	1
3. Description	1
4. Typical Application Circuits	1
5. Table of Contents	2
6. Block Diagram	3
7. Specifications	4
7.1. Absolute Maximum Ratings ⁽¹⁾ (with respect to Source (pad) unless noted)	4
7.2. Recommended Operating Conditions	4
7.3. ESD Ratings	4
7.4. Thermal Resistance	4
7.5. Electrical Characteristics	5
7.6. Typical Performance	7
8. Pin Configurations and Functions	10
8.1. GaN "Single" DPAK-4L	10
9. Functional Description	11
9.1. GaN Power IC Connections and Component Values	11
9.2. UVLO Mode	12
9.3. Normal Operating Mode	12
9.4. Low Power Standby Mode and Sleep Mode	13
9.5. GaN Technology Loss-Less Current Sensing	14
9.6. Over Temperature Protection (OTP)	16
9.7. Drain-to-Source Voltage Considerations	16
9.8. GaN For High Side Application	17
10. PCB Layout Guidelines	18
11. Package outline	20
12. Tape and Reel Dimensions	22
13. Ordering Information	23
14. Revision History	24

6. Block Diagram



Notes:

- GND connection for the IC is to the die pad.
- CS is the analog test output.

7. Specifications

7.1. Absolute Maximum Ratings ⁽¹⁾ (with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{DS}	Drain-to-Source Voltage	-7 to +700	V
V_{TDS}	Transient Drain-to-Source Voltage ⁽²⁾	800	V
V_{CC}	Supply Voltage	30	V
V_{CS}	CS Pin Voltage	5.3	V
PWM	OUTH Output Pin Voltage	-0.6V~V _{cc}	V
I_D	120 mΩ Version Continuous Drain Current (@ T _C = 25°C)	13.6	A
I_D	120 mΩ Version Continuous Drain Current (@ T _C = 100°C)	8.6	A
I_D PULSE	120 mΩ Version Pulsed Drain Current (10 μs, T _J = 125°C)	17.2	A
T _J	Operating Junction Temperature	-55 to 150	°C
T _{STOR}	Storage Temperature	-55 to 150	°C

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS(TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS(TRAN)}$ rating allows for repetitive events that are <400ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 9.7 for detailed recommended design guidelines.

7.2. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V _{CC}	Supply Voltage	10.5		24	V
VPWM	PWM input pin voltage	0	5	V _{cc}	V

7.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001)	1,500	V
CDM	Charged Device Model (per JS-002)	1,000	V

7.4. Thermal Resistance

SYMBOL	PARAMETER	TYP (120 mΩ)	UNITS
$R_{\theta JC}^{(1)}$	Junction-to-Case	4.41	°C/W
$R_{\theta JA}^{(1)}$	Junction-to-Ambient	47.57	°C/W

(1) R_{θ} measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

7.5. Electrical Characteristics

Typical conditions: $V_{DS} = 400\text{ V}$, $V_{CC} = 15\text{ V}$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $I_D = I_{TEST}^{(2)}$ (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} and V_{DD} Supply Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Turn-On Threshold		9		V	
V_{CCUV-}	V_{CC} UVLO Falling Turn-Off Threshold			6.2	V	
$I_{QCC-STBY}$	V_{CC} Standby Current		50		μA	Standby
I_{CCO}	V_{CC} Operating Current		500		μA	PWM high
$I_{STARTUP}$				10	μA	$V_{CC} = 24\text{ V}$
$t_{WAKE_UV}^{(1)}$	Wake Up Delay from UVLO Mode		35		μs	$V_{CC} = 0 \rightarrow 15\text{ V}$ during $1\mu\text{s}$ PWM tie to V_{CC}
I_{CC-SW}	V_{CC} Switching Current, $120\text{ m}\Omega$		1.2		mA	$F_{SW} = 500\text{ kHz}$, $V_{DS} = \text{Open}$
Input Characteristics (PWM pin)						
V_{PWM_H}	PWM Pin Logic High Threshold			2.7	V	
V_{PWM_L}	PWM Pin Logic Low Threshold	1.1			V	
$V_{PWM-HYS}$	PWM Pin Input Logic Hysteresis		0.6		V	
Sleep mode Characteristics						
t_{WAKE_Sleep}	Wake up delay time from Sleep mode			1.1	μs	From PWM high
t_{TO_Sleep}	Time Out Delay Entering Sleep Mode		11		ms	From PWM low
Standby Mode Characteristics						
t_{TO_STBY}	Time Out Delay Entering Standby Mode		75		μs	
t_{WAKE_STBY}	Wake Up Delay Time from Standby Mode			350	ns	
Current Sense Characteristics (CS pin)						
I_{CS}	CS Pin Output Current	1.16	1.25	1.34	mA	$V_{PWM} = 5\text{ V}$, $I_{DS} = .5 * I_{DSMAX}$
$t_{CSDLY10}^{(1)}$	CS Pin Delay from $I_{DS}=10\%$ rated current to $V_{CS}=10\%$ of desired full-scale voltage		62		ns	0.25 μs from 0 to I_{Dmax} $R_{CS}=400\Omega$

Electrical Characteristics (cont.)

Typical conditions: $V_{DS} = 400\text{ V}$, $V_{CC} = 15\text{ V}$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $I_D = I_{TEST}^{(2)}$ (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Over Temperature Protection						
$T_{OTP+}^{(1)}$	OTP Shutdown Threshold		160		$^{\circ}\text{C}$	
T_{OTP_HYS}	OTP Restart Hysteresis		65		$^{\circ}\text{C}$	

Electrical Characteristics (cont.)

Typical conditions: $V_{DS} = 400\text{ V}$, $V_{CC} = 15\text{ V}$, $T_{AMB} = 25\text{ }^{\circ}\text{C}$, $I_D = I_{TEST}^{(2)}$ (unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
CYPG6148C GaN FET Characteristics (120 mΩ version)						
I_{DSS}	Drain-Source Leakage Current		0.15	25	μA	$V_{DS} = 650\text{ V}$, $V_{PWM} = 0\text{ V}$
I_{DSS}	Drain-Source Leakage Current		32		μA	$V_{DS} = 650\text{ V}$, $V_{PWM} = 0\text{ V}$, $T_C = 150\text{ }^{\circ}\text{C}$
$R_{DS(ON)}$	Drain-Source Resistance		120	168	$\text{m}\Omega$	$V_{PWM} = 5\text{ V}$, $I_D = 4.3\text{ A}$
V_{SD}	Source-Drain Reverse Voltage		3.5	5	V	$V_{PWM} = 0\text{ V}$, $I_{SD} = 4.3\text{ A}$
Q_{OSS}	Output Charge		18.9		nC	$V_{DS} = 400\text{ V}$, $V_{PWM} = 0\text{ V}$
Q_{RR}	Reverse Recovery Charge		0		nC	
C_{OSS}	Output Capacitance		19.4		pF	$V_{DS} = 400\text{ V}$, $V_{PWM} = 0\text{ V}$
$C_{O(er)}^{(3)}$	Effective Output Capacitance, Energy Related		30.2		pF	$V_{DS} = 400\text{ V}$, $V_{PWM} = 0\text{ V}$
$C_{O(tr)}^{(4)}$	Effective Output Capacitance, Time Related		47.3		pF	$V_{DS} = 400\text{ V}$, $V_{PWM} = 0\text{ V}$

1) Guarantee by design

(2) $I_{TEST} = 2\text{ A}$

(3) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(4) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

7.6. Typical Performance

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

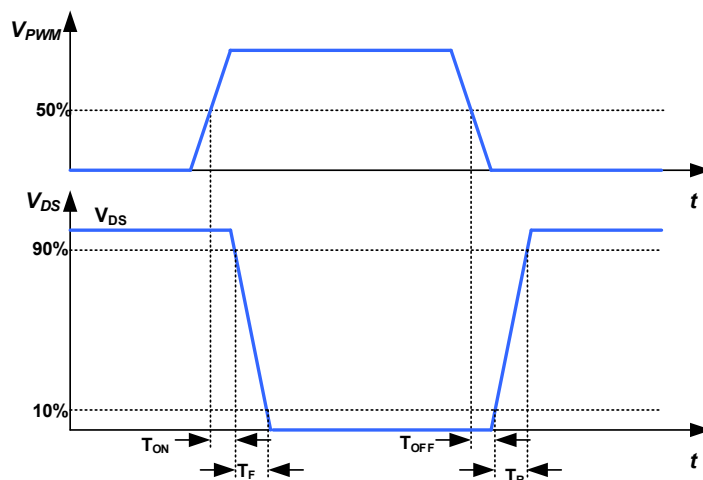


Figure 1. Inductive Switching Test Circuit

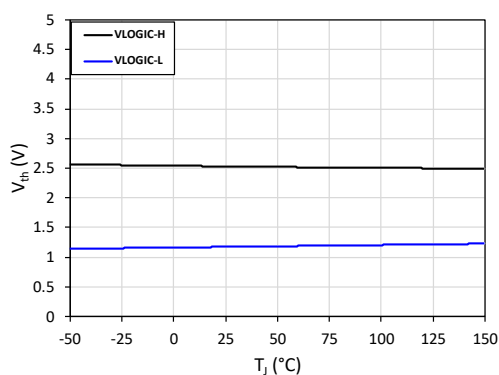


Figure 2. $V_{\text{LOGIC-H}}$ and $V_{\text{LOGIC-L}}$ vs. junction temperature (T_J)

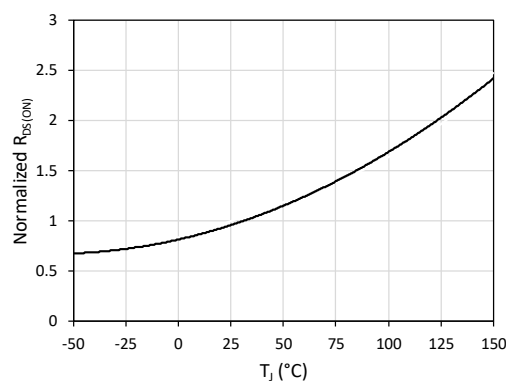


Figure 3. Normalized on-resistance ($R_{\text{DS(ON)}}$) vs. junction temperature (T_J)

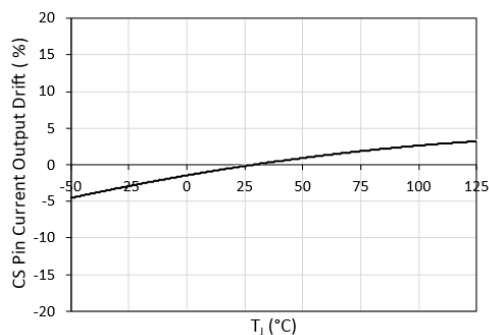


Figure 4. CS Pin Current Output Drift vs. case temperature (T_C)

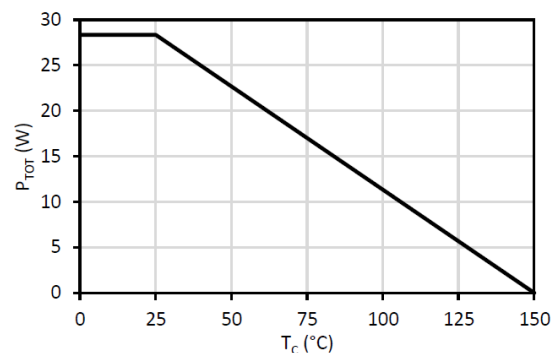


Figure 5. Power dissipation (P_{TOT}) vs. case temperature (T_C)

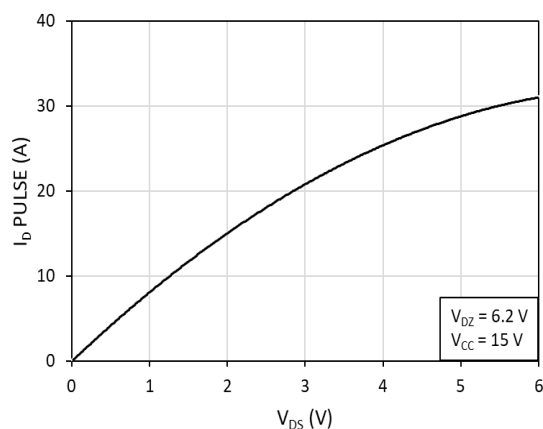
Typical Performance (cont.)


Figure 6. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at $T = 25\text{ }^{\circ}\text{C}$

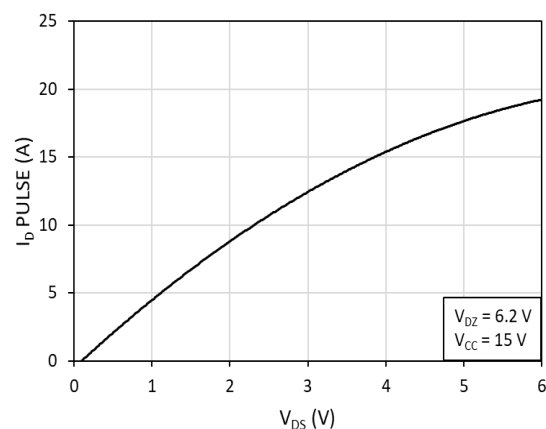


Figure 7. Pulsed Drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at $T = 125\text{ }^{\circ}\text{C}$

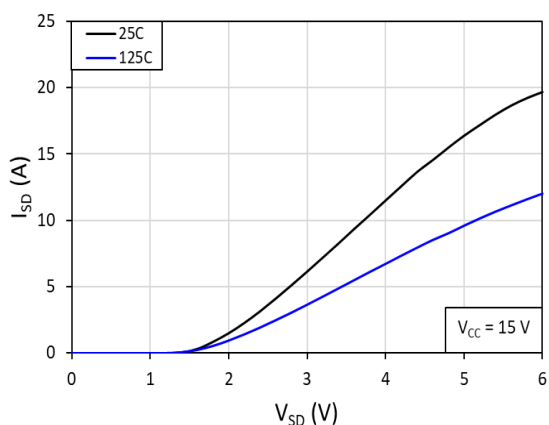


Figure 8. Source-to-drain reverse conduction voltage

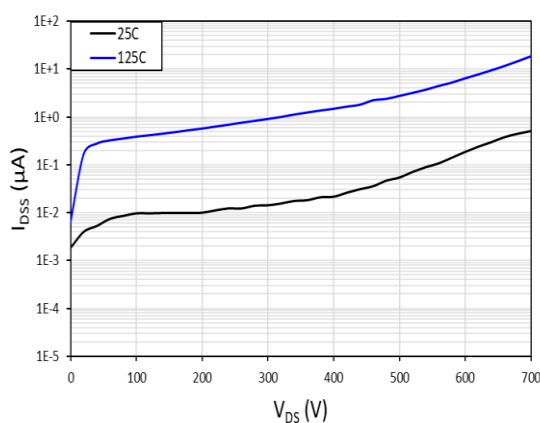


Figure 9. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

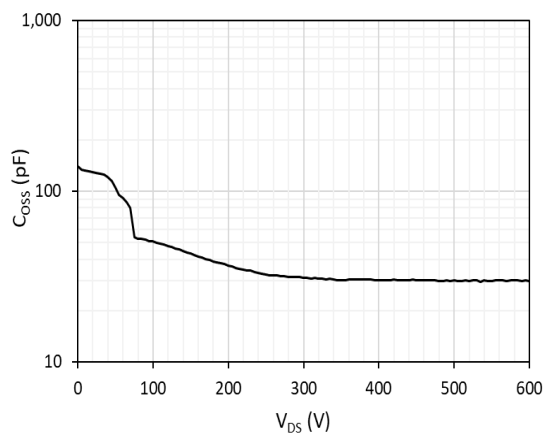


Figure 10. Output capacitance (C_{OSS}) vs. drain-to-source voltage (V_{DS})

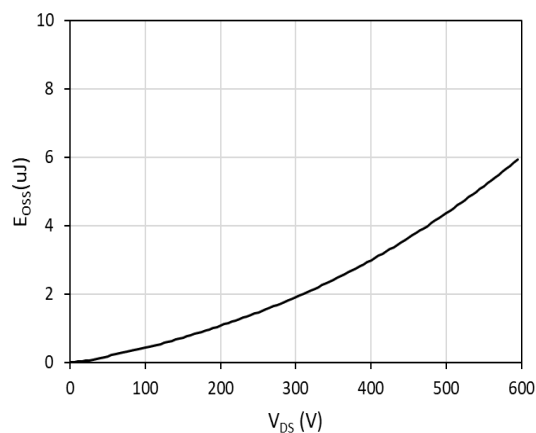


Figure 11. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

Typical Performance (cont.)

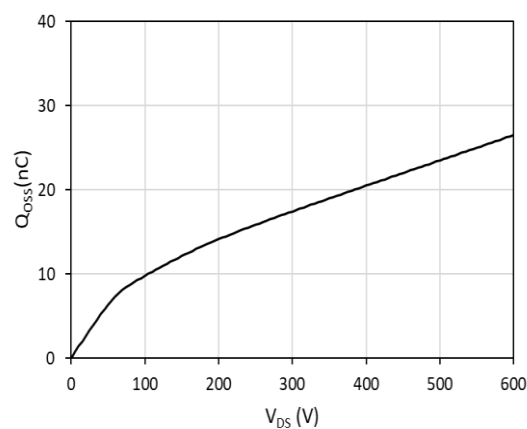


Figure 12. Charge stored in output capacitance (QOSS) vs. drain-to-source voltage (VDS)

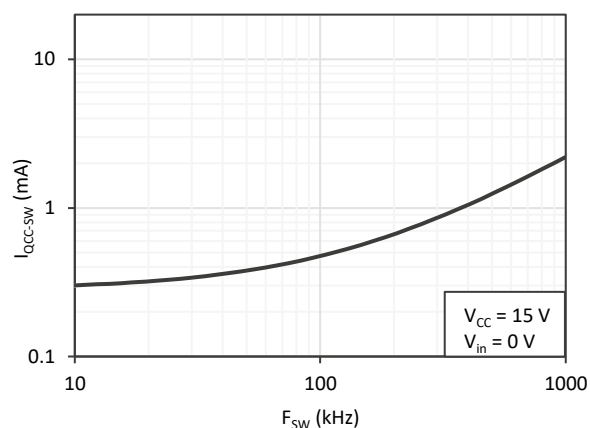


Figure 13. VCC operating current (I_{QCC-SW}) vs. switching frequency

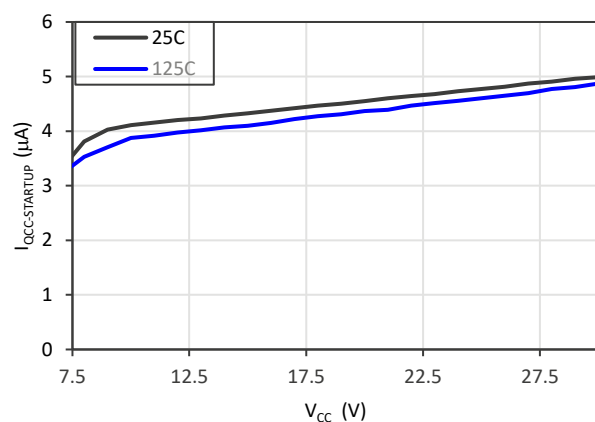


Figure 14. VCC startup current ($I_{QCC-startup}$) vs. Supply Voltage (VCC)

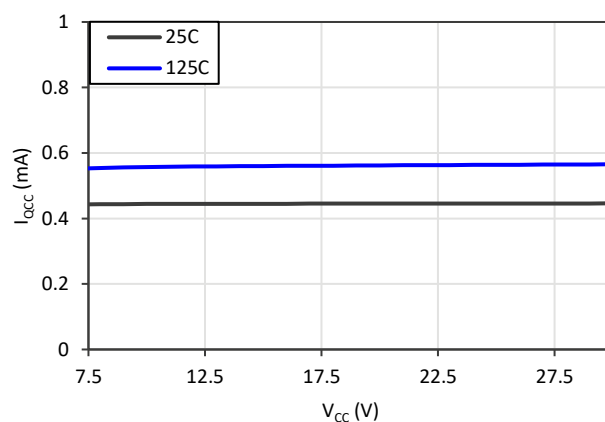


Figure 15. VCC quiescent current vs. Supply Voltage (VCC)

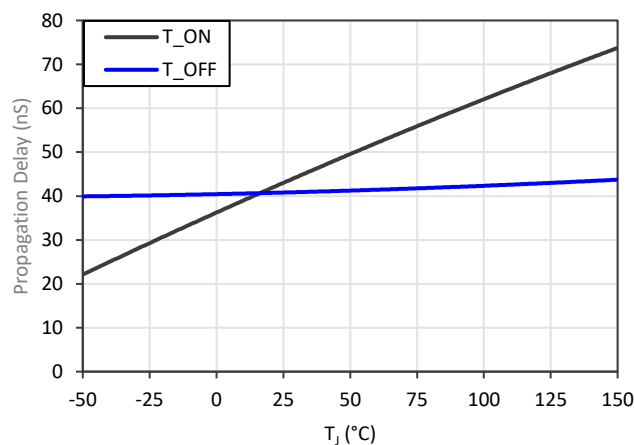


Figure 16. CP01 Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J)

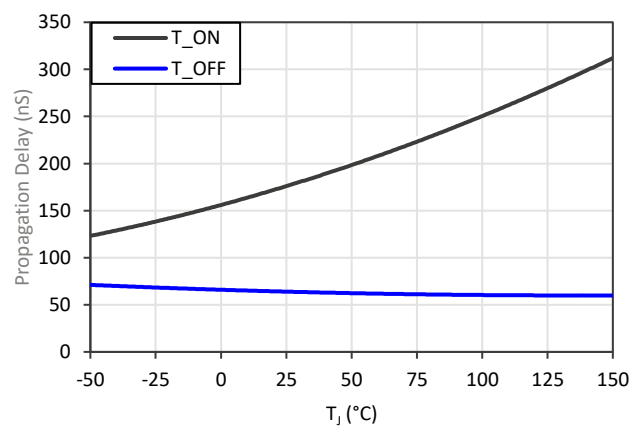


Figure 17. CQ01 Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J)

8. Pin Configurations and Functions

8.1. GaN "Single" DPAK-4L

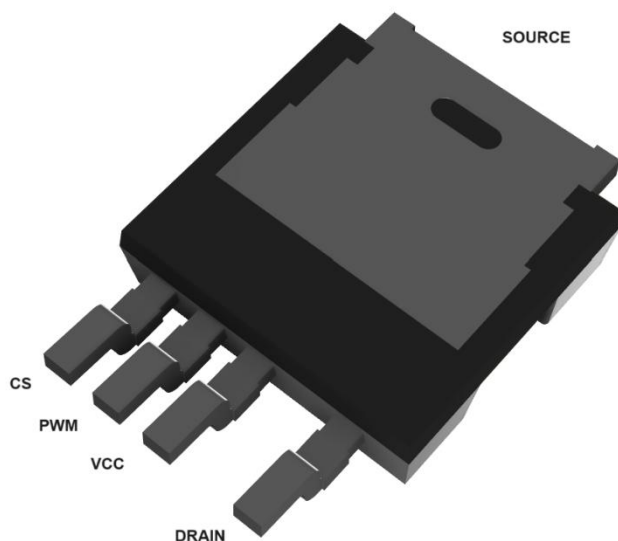


Figure 18. Package Bottom View

Pin		I/O ⁽¹⁾	Description
Number	Symbol		
1	Drain	P	Drain of power FET.
2	VCC	P	IC supply voltage.
3	PWM	I	PWM input.
4	CS	O	GaN FET I _{DS} current sensing set pin. Internal current source and external resistor sets current measurement level. External resistor reference is SGND.
SOURCE	GND	G	Source of power FET & IC supply ground. Metal pad on bottom of package.

Note 1: I = Input, O = Output, P = Power, G = Ground, T = Test Mode

9. Functional Description

The following functional description contains additional information regarding the IC operating modes and pin functionality. Please refer to the State Diagram for additional details.

9.1. GaN Power IC Connections and Component Values

The typical connection diagram for this GaN Power IC is shown in Figure 19. The IC pins include drain of the GaN power FET (D), source of the GaN power FET (S), IC supply (V_{CC}), PWM input (PWM), and current sensing output (CS). The external components around the IC include V_{CC} filter capacitor (C_{VCC}) connected between V_{CC} pin and S pin, a current sense amplitude set resistor (R_{SET}) connected between CS pin and S.

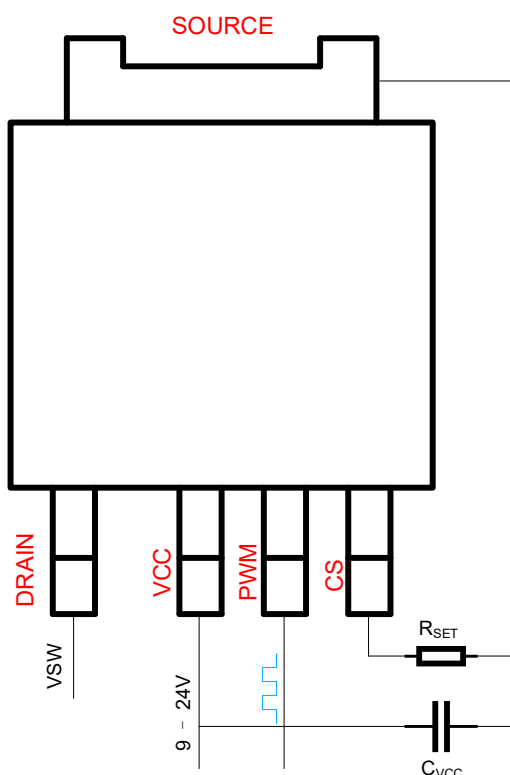


Figure 19. IC connection diagram

The following table (Table 1) shows the recommended component values (typical only) for the external components connected to the pins of this GaN power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.1	μF
R_{SET}	Current sense amplitude set resistor	Depends on system design (See Section 9.5 Equation 1)	Ω

Table 1. Recommended component values (typical only).

9.2. UVLO Mode

This GaN Power IC includes under-voltage lockout (UVLO) circuits for properly disabling all the internal circuitry when V_{CC} is below the V_{CCUV+} threshold (8.5V, typical). During UVLO Mode, the internal gate drive and power FET are disabled and V_{CC} consumes a low quiescent current which is less than 10uA. As the V_{CC} supply voltage increases (Figure 20) and exceeds V_{CCUV+} , the IC enters Normal Operating Mode when PWM goes high. The gate drive is enabled and the control signal at the PWM input turns the internal GaN power FET on and off normally. During system power off, when V_{CC} decreases below the V_{CCUV-} threshold (5.5, typical), the gate drive is disabled, and the IC enters UVLO Mode.

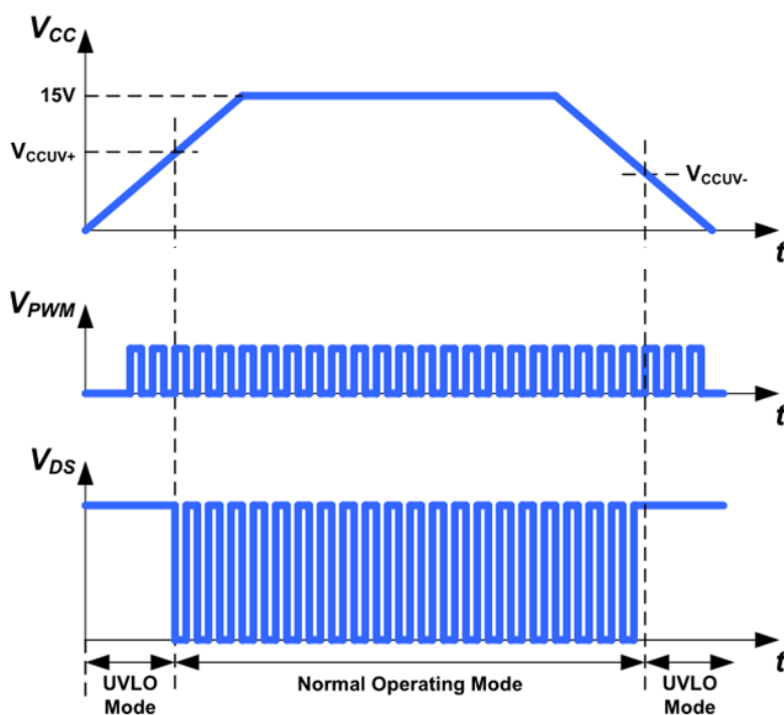


Figure 20. UVLO Mode and Normal Operating Mode Timing Diagram

9.3. Normal Operating Mode

During Normal Operating Mode, all the internal circuit blocks are active. V_{CC} is above 9.5V, the internal gate drive and power FET are both enabled. The external PWM signal at the PWM pin determines the frequency and duty-cycle of the internal gate of the power FET. As the PWM voltage toggles above and below the rising and falling input thresholds (2.7V and 1.1V), the internal power FET toggles on and off (Figure 21). The drain of the power FET then toggles between the source voltage (power ground) and a higher voltage level (700V, max), depending on the external power conversion circuit topology. During each on-time, the CS pin outputs a voltage signal from the internal loss-less current sensing circuit. This circuit measures the current flowing in the GaN power FET without the need for an external current sensing resistor (see section 9.5 GaN Technology Loss-Less Current Sensing).

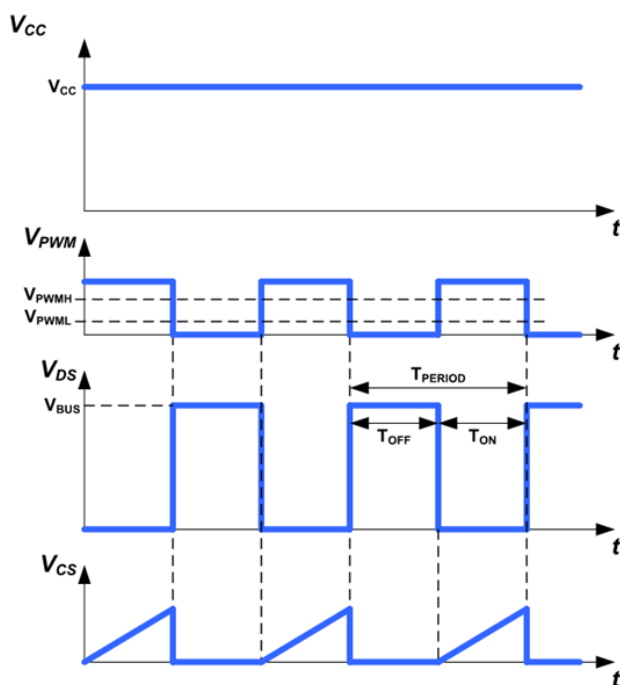


Figure 21. Normal Operating Mode Timing Diagram (PWM input)

9.4. Low Power Standby Mode and Sleep Mode

This GaN Power IC includes an autonomous Low Power Standby Mode for disabling the IC and reducing the V_{CC} current consumption. During Normal Operating Mode, the PWM pin toggles high and low to turn the GaN power FET on and off. If the input pulses at the PWM pin stop and stay below the lower V_{PWL} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY} , 75 μ sec, typical), then the IC will automatically enter Low Power Standby Mode (Figure 22). This will disable the gate drive and internal current sense circuitry and reduce the V_{CC} supply current to a low level (50 μ A, typical). If PWM pin continues to stay below the lower V_{PWL} turn-off threshold for the duration of the internal timeout sleep delay (t_{TO_SLEEP} , 10msec, typical), then the IC will automatically enter Low Power Sleep Mode (Figure 22). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to less than 10 μ A. When the PWM pulses restart, the IC will wake up with another wake-up delay (less than 200ns from standby mode or less than 1 μ s from Sleep mode) at the first rising edge of the PWM input and enter Normal Operating Mode again.

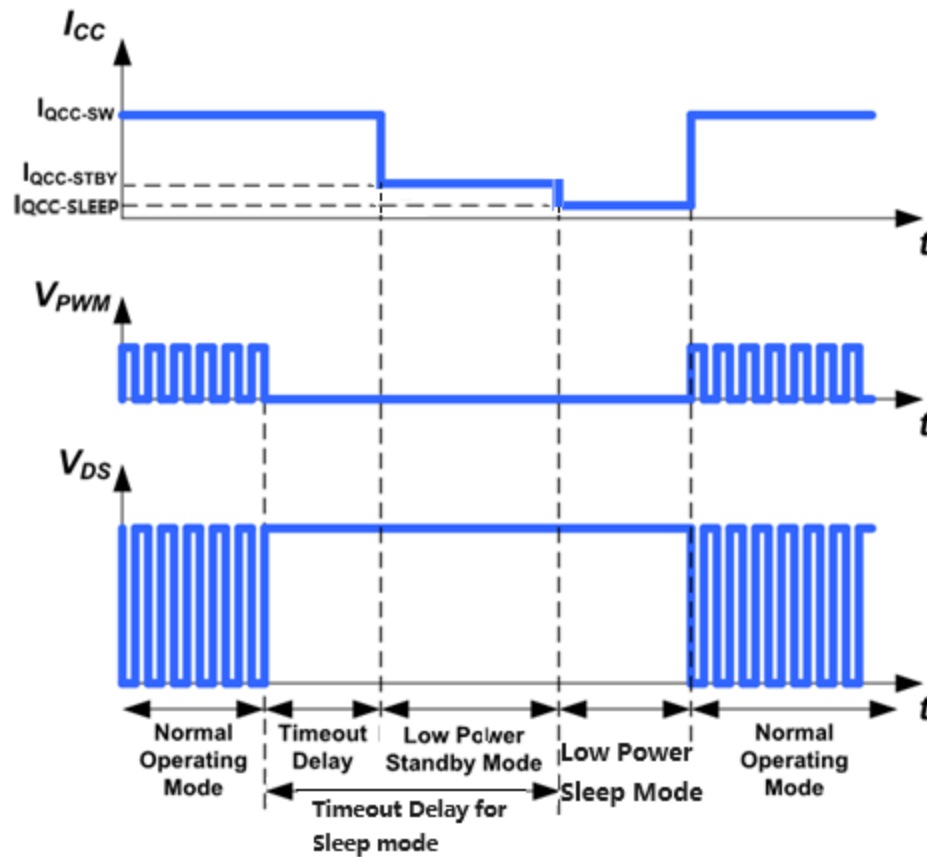


Figure 22. Sleep Mode Operating Timing Diagram

9.5. GaN Technology Loss-Less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. Existing current sensing solutions include placing a current sensing resistor in between the source of the power FET and PGND. This resistor method increases system conduction power losses, creates a hotspot on the PCB, and lowers overall system efficiency. To eliminate this external resistor and hotspot, and increase system efficiency, this IC includes GaN technology for integrated and accurate loss-less current sensing. The current flowing through the internal GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the GND pin and is used to set the amplitude of the CS pin voltage signal (Figure 23). This allows for the CS pin signal to be programmed to work with different controllers with different current sensing input thresholds.

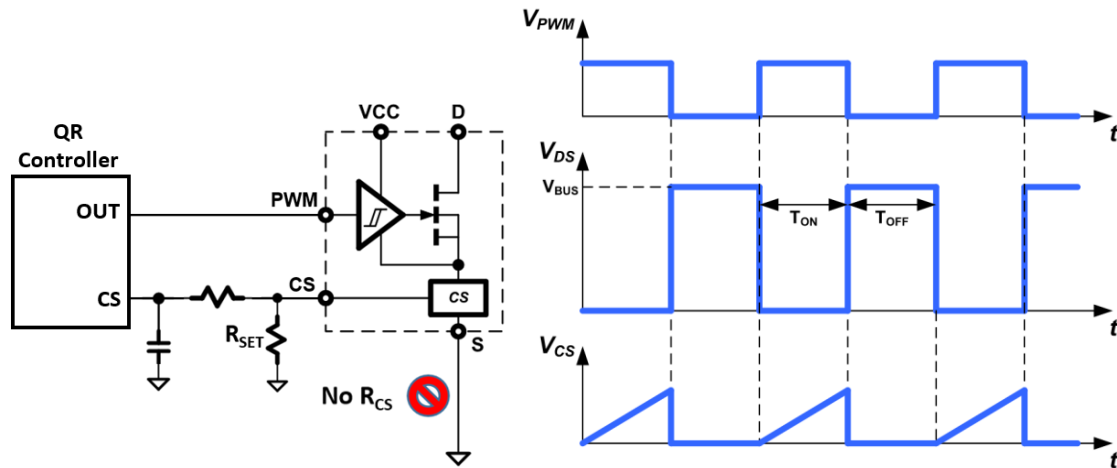


Figure 23. Current sensing circuit and timing diagram

When comparing GaN technology versus existing external resistor sensing method (Figure 24), the total ON resistance, $R_{ON(TOT)}$, can be substantially reduced. For a 65W high-frequency QR flyback circuit, for example, $R_{ON(TOT)}$ is reduced from 240m to 120m. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system.

External Resistor Sensing Method

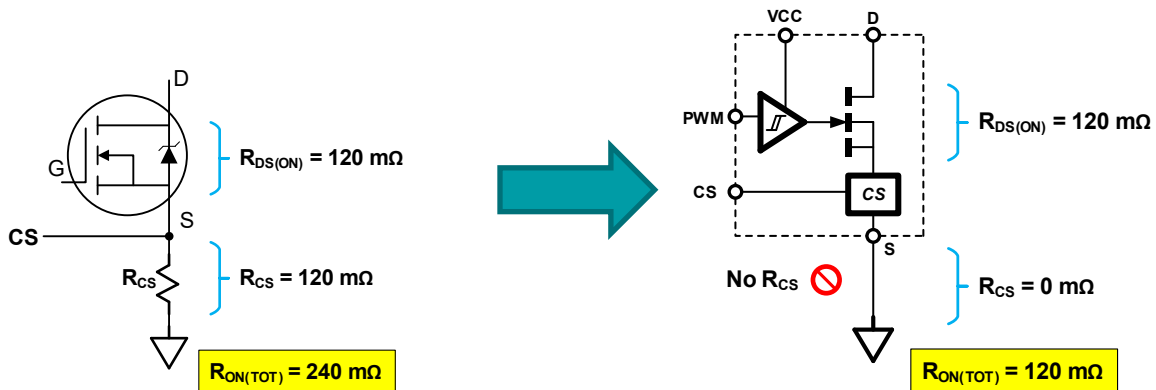


Figure 24. External resistor sensing vs. integrated GaN sensing technology

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry, to generate the equivalent R_{SET} resistor value. This R_{SET} value will then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$R_{SET} * I_{CS} = R_{CS} * I_{DS}$$

$$I_{CS_Ratio} = \frac{I_{DS}}{I_{CS}}$$

$$R_{SET} = I_{CS_Ratio} * R_{CS}$$

Equation 1. R_{SET} resistor value equation

PartNumber	CYPG6148C
I_{CS_ratio}	4968

9.6. Over Temperature Protection (OTP)

This GaN Power IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165°C, typical) then the IC will latch off safely. When T_J decreases again and falls below the internal T_{OTP-} threshold (95°C, typical), then the OTP latch will be reset. Until then, internal OTP latch guaranteed to remain in the correct state while V_{CC} is greater than 5V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Figure 25). V_{CC} will increase above the rising UV+ threshold and the controller turn on again and deliver PWM pulses again.

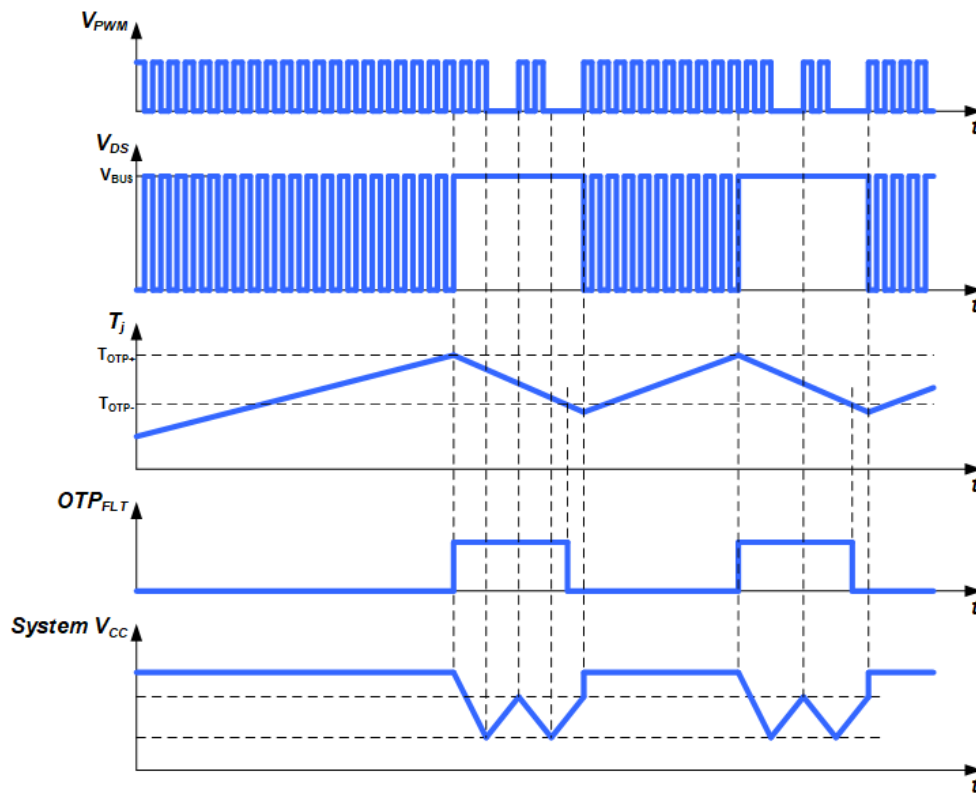


Figure 25. OTP threshold timing diagram

9.7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Figure 26. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE} . The clamp circuit should be designed to control the magnitude of V_{SPIKE} . After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Figure 26 as V_{DS-OFF} .

- For repetitive events, 80% derating should be applied from $V_{DS(TRAN)}$ rating (800V) to 640V max under the worst-case operating conditions.

- It is recommended to design the system such that V_{DS-OFF} is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the V_{DS-OFF} derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive V_{SPIKE} durations $< 100 \mu s$. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are $< 400 ns$, with 80% derating required (for example repetitive leakage inductance spikes).

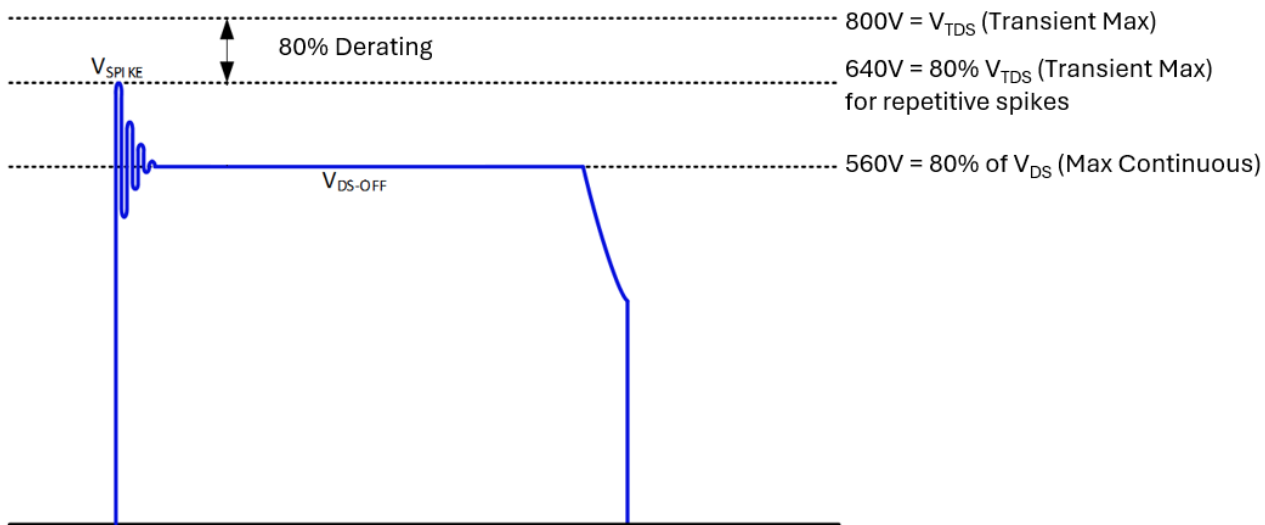


Figure 26. QR flyback drain-to-source voltage stress diagram

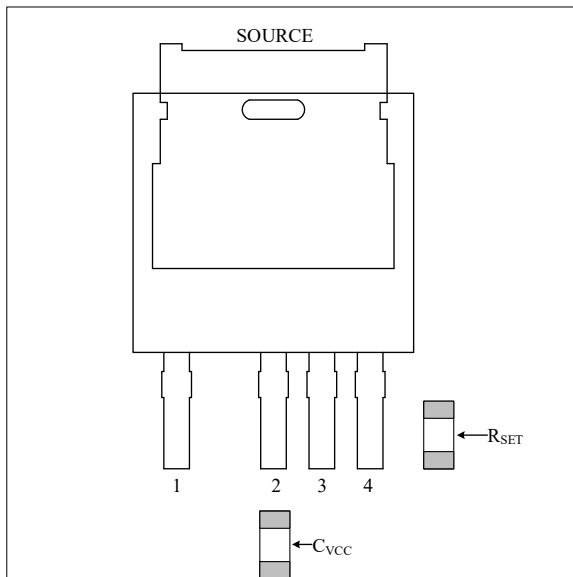
9.8. GaN For High Side Application

The wake-up time from UVLO for the internal driver has a 35 μs (typ) delay. This must be considered by the controller when designed for high side applications where power is supplied by a bootstrap circuit. An application note, *Design Guide for Integrated Driver GaN Products Used in LLC Circuits* provides additional detail and design recommendations.

10. PCB Layout Guidelines

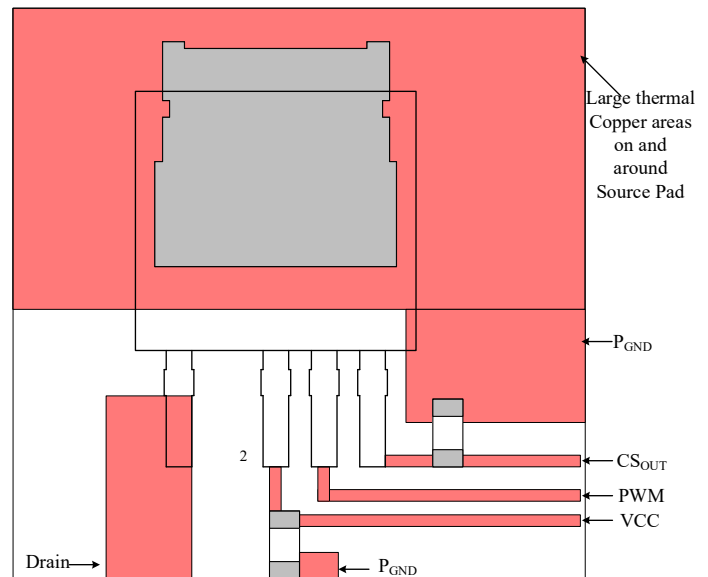
The design of the PCB layout is critical for good noise immunity, sufficient thermal management, and proper operation of the IC. A typical PCB layout example is shown as follows. The following rules should be followed carefully during the design of the PCB layout:

- 1) Place IC filter and programming components directly next to the IC. These components include (CVCC, RCS). Reference all these components to the GND pin.
- 2) Do not run power GND currents through signal GND!
- 3) For best thermal management, place thermal vias in the source pad area to conduct the heat out through the bottom of the package and through the PCB board to other layers.
- 4) Use large PCB thermal planes (connected with thermal vias to the source pad) and additional PCB layers to reduce IC temperatures as much as possible.



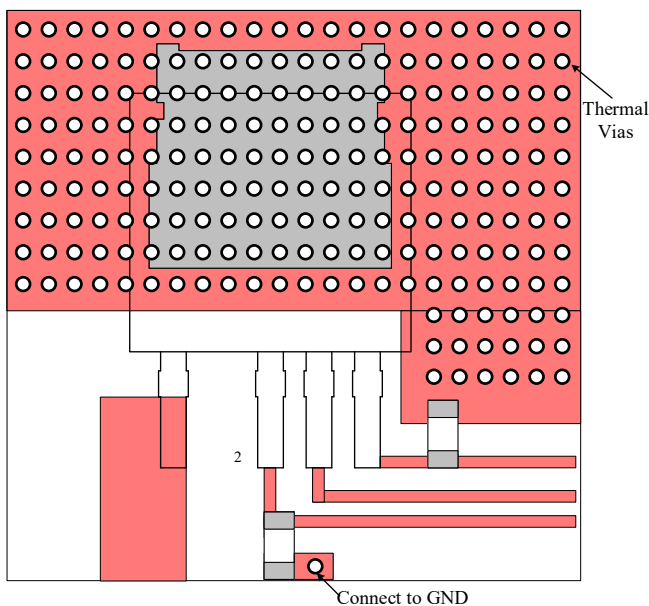
Step 1. Place GaN IC and components on PCB.

Place components as close as possible to IC



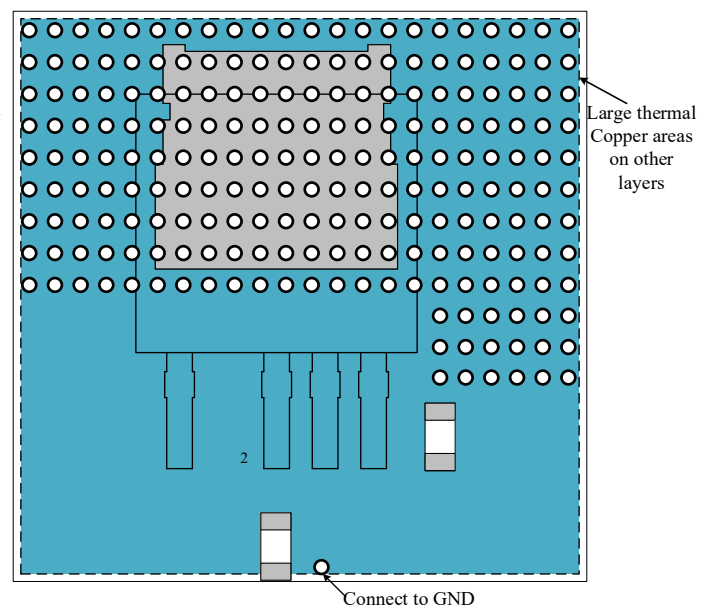
Step 2. Route all connections on single layer.

Make large copper areas on and around Source pad



Step 3. Place many thermal vias inside source pad and inside source copper areas.

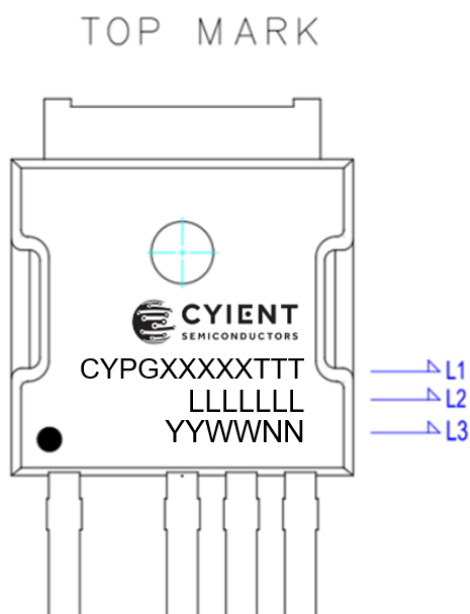
(dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall 1mil)



Step 4. Place large copper areas on other layers.

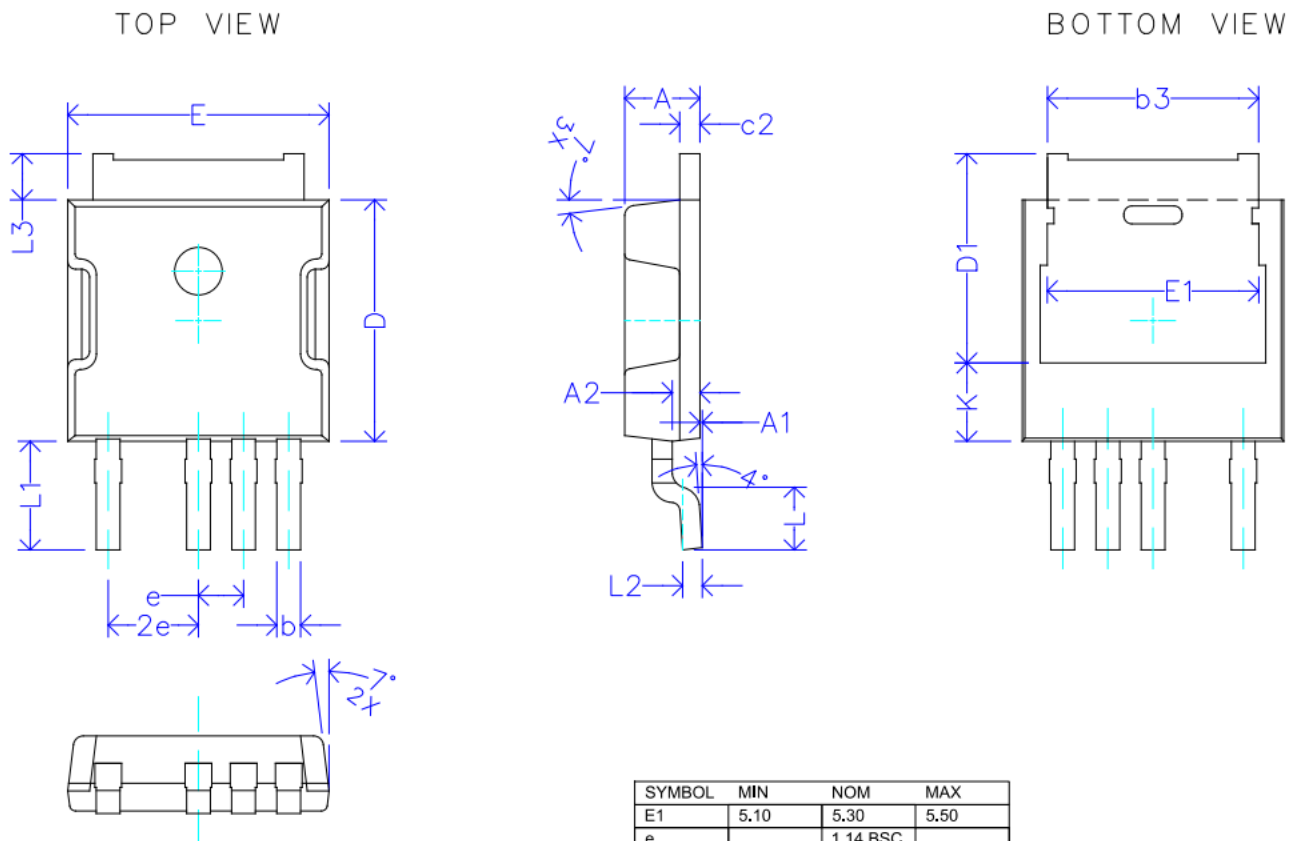
Make all thermal copper areas as large as possible

11. Package outline



Marking Line	Marking Characters	Description
L1	CYPGXXXXX	Base part number Example: CYPG6148C
	TTT	Optional Trim Code Example: Q01
L2	LLLLLLL	Lot Number Maximum 7 characters
L3	YY	Year Code: Last 2 digits of year Example: 2026, YY=26
	WW	Week Code: 01 – 53
	NN	Supplier Site Code

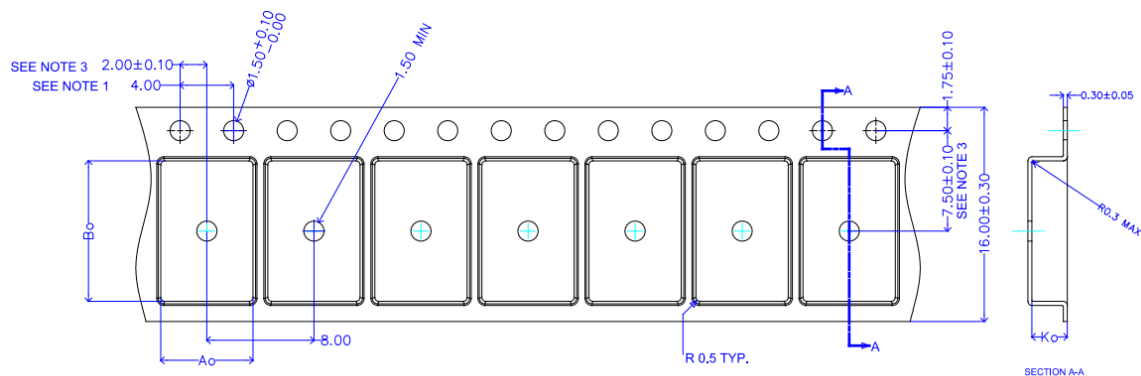
11. Package outline (cont.)



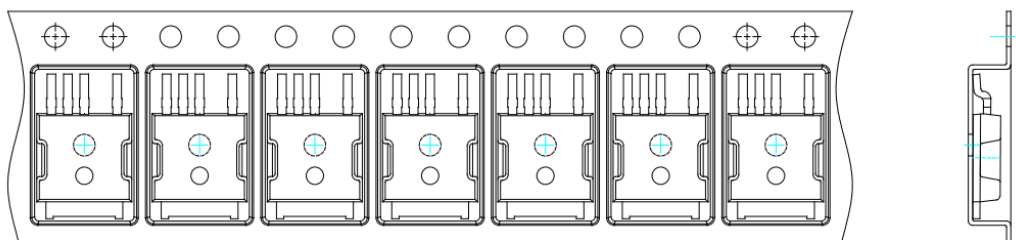
SYMBOL	MIN	NOM	MAX
A	1.80	1.90	2.00
A1	0.00	-	0.20
A2	0.60	0.70	0.80
b	0.508	0.60	0.711
b3	5.21	-	5.46
c2	0.41	0.508	0.61
D	6.00	6.10	6.22
D1	4.90	-	-
E	6.40	6.60	6.73

SYMBOL	MIN	NOM	MAX
E1	5.10	5.30	5.50
e		1.14 BSC	
L	1.34	1.585	1.77
L1		2.743 REF	
L2	0.41	0.508	0.61
L3	0.88	-	1.28
K	1.98	-	-
Package Draft Angles		5-9 degrees	
Foot Angle		0-8 degrees	
Gauge Plane for L		0.508	
Notes :			
1. All dimensions in mm.			
2. Reference JEDEC TO-252F VAR AD			
3. 100% Sn Plating			

12. Tape and Reel Dimensions



Notes	
Ao	6.9
Bo	10.50
Ko	2.65
1. 10 sprocket hole pitch cumulative tolerance ± 0.2	
2. Camber in compliance with EIA 481	
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.	



13. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Note	Package	MSL Rating	Packing (Tape & Reel)
CYPG6148CQ01	-55 °C to +150 °C T _J	-55 °C to +150 °C T _{STOR}	Isolated topology	DPAK-4L	3	2,000: 13" Reel
CYPG6148CP01	-55 °C to +150 °C T _J	-55 °C to +150 °C T _{STOR}	Non-isolated topology	DPAK-4L	3	2,000: 13" Reel

14. Revision History

Date	Status	Notes
June 2026	Final version	First publication

Additional Information

DISCLAIMER Cyient Semiconductors Inc. (Cyient Semiconductors) reserves the right to modify the products and/or specifications described herein at any time and at Cyient Semiconductors' sole discretion. All information in this document, including descriptions of product features and performance, is subject to change without notice. Performance specifications and the operating parameters of the described products are determined in the independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied. This document is presented only as a guide and does not convey any license under intellectual property rights of Cyient Semiconductors or any third parties.

Cyient Semiconductors' products are not intended for use in applications involving extreme environmental conditions or in life support systems.

Products supplied under Cyient Semiconductors Terms and Conditions.

Cyient Semiconductors and associated logos are registered trademarks of Cyient Semiconductors.

IMPORTANT NOTICES AND DISCLAIMERS

EXCEPT TO THE EXTENT THAT INFORMATION IN THIS DATA SHEET IS EXPRESSLY AND SPECIFICALLY WARRANTED IN WRITING BY CYIENT SEMICONDUCTORS (“**CYIENT SEMICONDUCTORS**”), EITHER PURSUANT TO THE TERMS AND CONDITIONS OF THE LIMITED WARRANTY CONTAINED IN CYIENT SEMICONDUCTORS’ STANDARD TERMS AND CONDITIONS OF SALE OR A WRITTEN AGREEMENT SIGNED BY AN AUTHORIZED CYIENT SEMICONDUCTORS REPRESENTATIVE, (1) ALL INFORMATION IN THIS DATA SHEET OR OTHER RELIABILITY AND TECHNICAL DATA, INCLUDING WITHOUT LIMITATION ANY DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION NOTES, OTHER DESIGN ADVICE OR TOOLS, SAFETY INFORMATION AND OTHER RESOURCES/MATERIALS, ARE PROVIDED “AS IS” AND WITH ALL FAULTS; AND (2) CYIENT SEMICONDUCTORS MAKES NO WARRANTIES OR REPRESENTATIONS AS TO ANY SUCH INFORMATION OR RESOURCES/ MATERIALS, IN THIS DATA SHEET OR OTHERWISE, AND HEREBY EXPRESSLY DISCLAIMS ALL WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

CUSTOMER RESPONSIBILITIES. This data sheet and other design resources and information provided by Cyient Semiconductors are intended only for technically trained and skilled developers designing with Cyient Semiconductors branded products (“**Products**”). Performance specifications and the operating parameters of Products described herein are determined in the independent state and may not perform the same way when installed in customer products. The customer (or other user of this data sheet) is solely responsible for (a) designing, validating and testing the products and systems in which Products are incorporated; (b) designing, validating and testing the application in which Products are incorporated; (c) ensuring the application meets applicable standards and any safety, security, regulatory or other requirements; (d) evaluating the suitability of Products for the intended application and the completeness of the information in this data sheet with respect to such application; (e) procuring and/or developing production firmware, if applicable; and (f) completing system qualification, compliance and safety testing, EMC testing, and any automotive, high-reliability or other system qualifications that apply.

NON-AUTHORIZED USES OF PRODUCTS. Except to the extent expressly provided in a writing signed by an authorized Cyient Semiconductors representative, Products are not designed, authorized or warranted for use in extreme or hazardous conditions; aircraft navigation, communication or control systems; aircraft power and propulsion systems; air traffic control systems; military, weapons, space-based or nuclear applications; life-support devices or systems, including but not limited to devices implanted into the human body and emergency medical equipment; or applications where product failure could lead to death, personal injury or severe property or environmental damage. The customer or other persons using Products in such applications without Cyient Semiconductors’ agreement or acknowledgement, as set forth in a writing signed by an authorized Cyient Semiconductors representative, do so entirely at their own risk and agree to fully indemnify and hold harmless Cyient Semiconductors, and its group companies/affiliates, from and against any damages resulting from or attributable to such improper and unauthorized use. In order to minimize risks associated with such applications, you should provide adequate design and operating safeguards.

CHANGES TO, AND USE OF, THIS DATA SHEET. This data sheet and accompanying information and resources are subject to change without notice. Cyient Semiconductors grants a limited, non-exclusive, and revocable license to use this data sheet and accompanying resources only for the development of an application that uses the Products described herein and subject to the notices and disclaimers set forth above. Any other use, reproduction or display of this data sheet or accompanying resources and information is strictly prohibited. No license, express or implied, is granted to any Cyient Semiconductors’ intellectual property right or to any third-party intellectual property right. Cyient Semiconductors disclaims any responsibility for, and you will fully indemnify and hold harmless Cyient Semiconductors, its affiliates and representatives against, any claims, damages, costs, losses and liabilities arising out of your use of this data sheet and any accompanying resources and information.

TERMS AND CONDITIONS. All purchases and sales of Products are subject to Cyient Semiconductors’ Standard Terms and Conditions of Sale, including the limited warranty contained therein, unless other terms and conditions have been agreed in a writing signed by an authorized Cyient Semiconductors representative. This data sheet, and Cyient Semiconductors’ provision of this data sheet or other information and resources, do not expand or otherwise alter those terms and conditions.

Products and related technical information may be subject to export control, sanctions, customs, and trade compliance laws and regulations. Customer is solely responsible for compliance with all applicable export control requirements and for obtaining any necessary authorizations prior to use, export, or transfer.

Cyient Semiconductors, the Cyient Semiconductors logos, and other Cyient Semiconductors marks used herein are trademarks or registered trademarks of Cyient Semiconductors or its affiliates. Other trademarks used herein are the property of their respective owners.

Copyright © 2026 Cyient Semiconductors Semiconductor Limited and affiliates. All rights reserved.